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10ES33

# Third Semester B.E. Degree Examination, December 2012

## Logic Design

Time: 3 hrs. Max. Marks:100

**Note:** ***Answer FIVE full questions, selecting at least TWO questions from each part.***



### PART – A

1 a. Define canonical Minterm form and canonical Maxterm form. **(05 Marks)**

b. Design a three-input, one output minimal two-level gate combinational circuit which has an output equal to 1 when majority of its inputs are at logic 1 and has an output equal to 0 when majority of its inputs are at logic 0. **(05 Marks)**

c. Minimize the following multiple output functions using K-MAP:

$f_1 = \sum m(0,2,6,10,11,12,13) + d(3,4,5,14,15)$

$f_2 = \sum m(1,2,6,7,8,13,14,15) + d(3,5,12)$ **(10 Marks)**

2 a. Use a K-Map to simplify that following functions:

i) $f(A,B,C,D) = (A+B+\overline{C})(\overline{B}+\overline{D})(\overline{A}+C)(B+C)$

ii) $f(A,B,C,D) = \pi(1,2,4,5,7,8,10,11,13,14)$ **(10 Marks)**

b. Find all the prime implicants of the function

$f(a,b,c,d) = \sum(7,9,12,13,14,15) + \sum d(4,11)$

Using Quine Mc Clusky algorithm. **(10 Marks)**

3 a. Reduce the given function using MEV technique:

i) $f = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C\,D + \overline{A}\,B\,\overline{C}\,\overline{D} + A\overline{B}\,\overline{C}\,D + ABCE + ABC\overline{E} + d(A\overline{B}CD + A\overline{B}\,CE)$

ii) $f = m_0 + m_1F + m_2 + m_4F + m_6(E+\overline{E}) + m_7F + m_{10}E$

$+ m_{12} + m_{15}F + d(m_5F + m_9\overline{F} + m_{11}\overline{E} + m_8E)$ **(10 Marks)**

b. Write the condensed truth table for a 4 to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index and obtain the minimal sum expressions for the outputs. **(06 Marks)**

c. Describe general working principle of decoder. **(04 Marks)**

4 a. Explain the working principle of four-bit parallel fast look ahead carry adder. **(10 Marks)**

b. Design a comparator to check if two n-bit numbers are equal. Configure this using cascaded stages of 1-bit comparators. **(10 Marks)**

### PART – B

5 a. With a neat diagram, explain the working of Master-Slave JK flip-flop along with waveforms. **(10 Marks)**

b. Explain switch debouncer using SR latch with waveforms. **(10 Marks)**

6 a. Explain universal shift register with the help of logic diagram, mode control table. **(10 Marks)**

b. Design and implement a divide-by-10 asynchronous counter using T FFS. **(10 Marks)**

7 a. Design and implement a synchronous BCD counter using J-K FFS. **(10 Marks)**

b. A sequential circuit has one input and one output state diagram is as shown in Fig.Q7(b). Design the sequential circuit with J-K flip-flop.

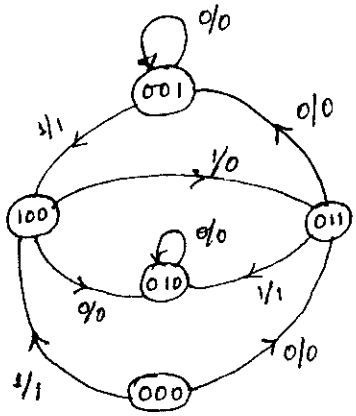


Fig.Q7(b) **(10 Marks)**

8 a. Design a sequence detector for the following sequence 1, 0, 1, 1, 1 with overlap. Write the state diagram and logic diagram. **(10 Marks)**

b. A sequential circuit has two flip-flops A and B, two inputs x and y, and an output z. The flip-flop input functions and the circuit output functions are as follows:

$J_A = x\,B + \bar{y}\,\bar{B}$; $K_A = x\,\bar{y}\,\bar{B}$

$J_B = x\,\bar{A}$; $K_B = x\,\bar{y} + A$

$z = xyA + \bar{x}\,\bar{y}\,B$

Obtain the logic diagram, state table and state equations, also state diagram. **(10 Marks)**

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